Specificati n Amendments

Amend the paragraph beginning on application page 7, line 27 and continuing on page 8 as follows:

The above-noted segmentation of the gate structure into the split gates 110, 112 provides an efficient mechanism for implementing gate isolation between adjacent transistors in the horizontal direction, i.e., in the direction of the x-axis in this example. More particularly, in this example, gates G1P and G1N are active and comprise the first inverter, i.e., Inverter 1, while the gates G3P and G3N are active and comprise the second inverter, i.e., Inverter 2. The gates corresponding to Inverter 1 and Inverter 2 are also denoted A1 and A2, respectively, in the figure. The gates G2P and G2N in this example are used as isolating gates. These gates electrically separate the transistor source and drain regions Z1 ~~and Z2~~ of Inverter 1 from the source and drain regions Z2 of Inverter 2 in the direction of the x-axis, in both the PFET and NFET regions. This isolation is achieved in this example by tying G2P to the upper supply voltage VDD and G2N to the lower supply voltage VSS as shown. The split gate structure comprising gates G2P and G2N prevents the shorting of the VDD supply voltage. As indicated above, this arrangement isolates the source and drain regions Z1 of the first inverter from the source and drain regions Z2 of the second inverter. Similar isolation techniques can be implemented using other arrangements involving the base transistor structure of FIG.1A.